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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/567,357 | 02/06/2006 | Kazuhito Tanaka | P29233 | 1320 |

52123 7590 03/25/2011

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| EXAMINER | |
|---|---|
| JOSEPH, DENNIS P | |
| ART UNIT | PAPER NUMBER |
| 2629 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 03/25/2011 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/567,357 | TANAKA ET AL. | |
| | Examiner | Art Unit | |
| | DENNIS P. JOSEPH | 2629 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09 March 2011*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-11,13,14,16 and 18-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13,14,16 and 18-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

**DETAILED ACTION**

1. This Office Action is responsive to amendments filed for application No. 10/567,357 on March 9, 2011. Claims 1-11, 13, 14, 16 and 18-23 are pending and have been examined.

## Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claim 1, 2, 5-7, 13, 14, 16 and 18-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubota et al. ( US 6,288,699 B1 ) in view of Yamagishi et al. ( US 2004/0012580 A1 ).

For **claim 1,** Kubota teaches a clock signal generator that generates a clock signal (Kubota, column 8, lines 1-2). Kubota teaches the use of a clock signal, therefore there must be a clock signal generator. Kubota also teaches a test signal generator (Kubota, column 9, lines 39-53). Kubota teaches a signal video data line (RGB signal) which is then used to generate a signal video data line (DAT). The use of a single line implies serial data and also, please note Figure 2 for a data driver to the pixels. Kubota also teaches a phase adjusting device that adjusts the phase of the clock signal (Kubota, column 9, lines 39-53). Kubota teaches generating detecting signals which are the same as test signals. Kubota also teaches a serial data generator that generates

serial data according to an image to be displayed (Kubota, column 7, lines 19-26, and figure 1); but

Kubota does not specifically teach a latch failure detector that includes a "latcher that latches the test signal generated by said test signal generator to detect the presence/absence of a latch failure in said data driver based on an output signal from said latcher", "a first storage device that stores the phase of the clock signal adjusted by said phase adjustor as an optimal phase, wherein said phase adjuster varies the phase of said clock signal to detect a phase range within which a latch failure does not occur, and stores, in said first storage device, a phase in a center of said detected phase range as said optimal phase during said adjustment period, and adjusts the phase of said clock signal to said optimal phase stored in said first storage device in the write period after said optimal phase is stored by said first storage device" and "an adjustment period including a sustain period during a sustain period during which light emission of the discharge cells selected in said write period is sustained", indicative of a plasma display panel which has "a plurality of discharge cells".

However, Kubota teaches a phase adjusting circuit meant to correct the phase difference between the data and the clock. This phase difference is the cause of a latch failure; therefore detecting a phase difference in the phase adjusting circuit is the same as detecting a latch failure and wherein the phase adjustment of the clock signal is only made if a phase of the serial data and the phase of the clock signal differ at least a predetermined amount such that a latch failure is detected (Kubota, column 9, lines 39-53, figure 1). Respectfully, the difference is semantics as to

summarize, Kubota also is concerned with differences in the phase difference between the signals. Therefore, the signals MON1 and MON2 are used to detecting an internal delay and there is further a delay detecting circuit for determining the phase difference between these signals, ( Kubota, Column 9, Lines 38-52 ). These two signals could be interpreted reasonably as being the claimed test signals and based on the results of the phase difference, it is obviously determined if an adjustment needs to be made (indicative of a failure). At this point, the phase adjustment section makes the appropriate correction. Please note that Kubota has several disclosures about the data driving circuitry, with the associated latches, so it is obvious that the interpreted test signals are measuring signals across these latches. As for the selected optimal value, as noted above, Kubota teaches of specifically finding the optimal value and one of ordinary skill in the art would realize that it the optimal value would be in the center of the adjustment signal to avoid the latch failure errors at the edges of the acceptable range. Please note KSR principles and case law cover optimization and that it is indeed obvious to optimize, especially given Kubota is concerned with finding the optimal range as well.

Furthermore, it is clear that this optimal value is stored so that it may be applied and furthermore, during the next phase, a new optimal value may be stored ( Column 4, Lines 11-14 and Column 9, lines 39-53 ). In any case, examiner asserts Official Notice to the use of a memories/storage units which are commonly used to store values that are needed at a future time, making the use of these a necessity.

As for the adjustment period including a sustain period in which light emission of the discharge cells is performed Kubota teaches of using an LCD and not a plasma embodiment. However, as Applicant has noted, a write period is a skin to a sustain period. Please note that it is well known to provide for this phase adjustment in a wide range of displays since clock signal issues are known in the art in general.

In the same field of endeavor, phase adjustments for clock signals, Yamagishi teaches of adjusting the clock timings to reliably latch data, ( Yamagishi, [0017]-[0018] ), which is similar to the purpose of Kubota. Yamagishi notes his invention can be implemented in a plasma display ( Yamagishi, [0015] ). As one of ordinary skill in the art would realize, the sustain period is akin to the writing period of an LCD and given the clock adjustments are done in both references, that Kubota's invention could be implemented in a plasma display during the sustain period to perform light emission of the discharge cells. Several KSR principles can be applied here, such as well known technique (given that plasma/LCD/etc have clock issues and seek to adjust/correct them) and simple substitution of parts (given that Kubota's driving method can be implemented in a plasma display panel without destroying it since the driving method is applied to Yamagishi's structure).

Therefore, it would be obvious to one of ordinary skill in the art to implement Kubota's invention in a plasma display, as taught by Yamagishi, with the motivation of the KSR principles and that Yamagishi suggests doing so himself, ( Yamagishi, [0015] ).

For **claim 2,** Kubota teaches a data driver that includes a plurality of data driver units (Kubota, figure 4).

For **claim 5,** Kubota teaches adjusting the phase of the clock signal at predetermined intervals (Kubota, column 14, lines 30-34).

For **claim 6,** Kubota teaches a phase adjusting period at intervals of a plurality of fields (Kubota, figure 10).

For **claim 7,** Kubota teaches that the phase adjustment period could include a plurality of adjustment periods (Kubota, column 11, lines 25-31). Kubota does not specifically state that the phase adjustment device would continue from the beginning of the next period; however, the examiner takes official notice that it is well known that if the phase adjustment devices are not finished in one adjustment period then it will continue from the beginning of the next period because the phase adjustment does complete without breaks in-between. The examiner also takes official notice that a Phase Locked Loop (PLL) will adjust the phase of a signal in multiple periods and the phase adjustment will continue from the beginning of the next period if it did not finish and it is well known in the art. It would have been obvious to one of ordinary skill in the art to modify Kubota's system with the known technique of the phase adjustment device would continue from the beginning of th next period since this would allow for the phase adjustment to be completed faster.

For **claim 13**, Kubota teaches a buffer in the device (Kubota, figure 1). It would have been obvious to use the buffer for the clock signal as well. Kubota also teaches a plurality of delay elements that sequentially delay said clock signal by a predetermined delay amount (Kubota, column 3 line 61 - column 4 line 6). Kubota also teaches a selector that selectively outputs a plurality of clock signals (Kubota, column 11, lines 5-24, and figure 7).

For **claim 14,** Kubota teaches a delay circuit (Kubota, figure 1 and 13, column 3, lines 61-67). It would have been obvious to add more delay circuits (or reuse the same delay circuit) if one wanted delay circuits with different number of delay amounts since such a modification may only require a mere addition or replication of the delay section. Kubota also teaches selecting delay circuit and providing clock signal to the circuit (Kubota, figure 1, item 12).

For **claim 16,** Kubota teaches a phase adjusting device that can detect that the phase of the adjusted clock signal is the optimal phase and finish the adjustment of the phase of the clock signal when it is detected that the phase of the clock signal is the optimal phase (Kubota, column 9, lines 39-53). Kubota teaches adjusting the phase to an optimum value; therefore the device must be able to detect the optimal phase.

For **claim 18,** Kubota teaches adjusting the phase of the clock to an optimum value which it has calculated (Kubota, column 9, lines 39-53). Therefore, it would have been obvious that in order to adjust the phase to an optimal value, the device must have the optimal value stored since it

was not provided the optimal value from an external source. Kubota also teaches that the phase adjustment may take longer than one adjustment period (Kubota, column 11, lines 25-31).

For **claim 19**, Kubota teaches of finding the optimal value (Kubota, column 9, lines 39-53) and using the rationale in Claim 1, it is clear that one of ordinary skill in the art would realize optimization would dictate selecting the center value to better avoid latch errors in the clock signals.

For **claim 20,** Kubota teaches adjusting the phase of the clock with respect to the serial data (Kubota, column 4, lines 15-22, and figure 7 and 14).

For **claim 21,** Kubota teaches adjusting the phase of the clock to an optimum value; therefore the device must be able to detect the optimal phase of the clock (Kubota, column 9, lines 39-53). Kubota also teaches adjusting the phase of the video signal (Kubota, column 4, lines 11-14). Therefore, it would have been obvious to adjust the phase of the video signal when the clock signal is optimal.

For **claim 22,** Kubota teaches adjusting the phase to an optimum value which it has calculated (Kubota, column 9, lines 39-53). Therefore, it would have been obvious that in order to adjust the phase to an optimal value, the device must have the optimal value stored since it was not provided the optimal value from an external source. Kubota also teaches adjusting the phase of either the video data or the clock (Kubota, column 4, lines 7-21). It is obvious that Kubota could

store the phase of both clock and video data since both can be adjusted to an optimal phase. Kubota teaches adjusting the phase when it does not affect the image display (Kubota, column 5, lines 46-58). Therefore, it would have been obvious to do so in the write period.

For **claim 23,** Kubota teaches adjusting the phase to an optimum value which it has calculated (Kubota, column 9, lines 39-53). Therefore, it would have been obvious that in order to adjust the phase to an optimal value, the device must have the optimal value stored since it was not provided the optimal value from an external source. Kubota also teaches adjusting the phase of either the video data or the clock (Kubota, column 4, lines 7-21). It is obvious that Kubota could store the phase of the both the clock and video data since both can be adjusted to an optimal phase. Kubota teaches adjusting the phase when it does not affect the image display (Kubota, column 5, lines 46-58). Therefore, it would have been obvious to do so in the write period. It also would have been obvious to use the last optimal value that was stored since no new value was detected. This is so because if no new value was detected then the memory should still contain the last optimal value.

4. **Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kubota et al. ( US 6,288,699 B1 ) in view of Yamagishi et al. ( US 2004/0012580 A1 ), as applied to Claim 1, further in view of Haines ( US 4,697,107 ).

For **claim 3,** Kubota does not teach an open drain output.

However, in the same field of endeavor, Haines teaches a plurality of latches with open-drain outputs (Haines, column 3, lines 31-36). Haines also teaches a plurality of wired-OR connections for those latches (Haines, column 3, lines 37-56).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kubota's phase adjustment with Haines's control circuit because open-drain outputs and wired-OR connections can simplify the circuit by requiring fewer components.

5. **Claim 4, 8, 10 and 11** rejected under 35 U.S.C. 103(a) as being unpatentable over Kubota et al. ( US 6,288,699 B1 ) in view of Yamagishi et al. ( US 2004/0012580 A1 ), as applied to Claim 1, further in view of Saito ( US 20010054924 A1).

For **claim 4,** Kubota does not teach alternating the test signal pulse every clock period; however, in the same field of endeavor, Saito teaches the test signal as an alternating pulse signal that is inverted every period of the clock (Saito, page 2, paragraph [0015]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kubota's phase adjustment with Saito's test signal because using a test signal that alternates every period could improve the accuracy of the phase adjustment by allowing the adjustment to occur more frequently.

For **claim 8,** Kubota teaches a latch failure detector that generates a latch failure detection signal indicating the presence/absence of the latch failure, based on a first test signal obtained by delaying said test signal and second test signal obtained by delaying said test signal (Kubota, column 4, lines 1-6 & lines 54-59, column 10 lines 26-32). It would have been obvious to delay the test signals block clock periods because this would have been a simply way to accurately delay the signals by a set period of time. Kubota teaches a detection section that detects the phase difference and a phase adjusting section that adjusts the phase according to an instruction sent from the detection section based on the result of the detection section. Kubota also teaches using two detection signals to detect the phase difference between the two. Kubota does not teach using the exclusive logical sum of the detection signals; however, in the same field of endeavor, Saito teaches taking the logical sum of delay control signals used to adjust the phase of a signal (Saito, figure 6). It would have been an obvious matter of design choice to take the exclusive logical sum because such a modification would only require a mere change of the logic gate used.

For **claim 10,** Kubota teaches a detection unit that notifies the phase adjusting unit to adjust the phase of a signal (Kubota, column 10, lines 26-31). Kubota does not teach a holder for the detection result.

However in the same field of endeavor, Saito teaches holding the result of the detection (Saito, page 3, paragraph [0041]). Saito also teaches flip-flop circuits to hold control signals (Saito,

page 6, paragraph [0084]). It is well known in the art that flip flop have reset inputs to reset the flip flop.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kubota with Saito because it could improve the accuracy of the phase adjustment.

For **claim 11,** Kubota teaches a detection unit that notifies the phase adjusting unit to adjust the phase of a signal (Kubota, column 10, lines 26-31). Kubota does not teach a holder for the detection result; however in the same field of endeavor, Saito teaches holding the result of the detection (Saito, page 3, paragraph [0041]). Saito also teaches flip-flop circuits to hold control signals (Saito, page 6, paragraph [0084]). It is well known in the art that flip flop have reset inputs to reset the flip flop. It is also obvious to have a reset signal generating circuit if one chose to use the reset input of a flip flop because it is necessary to generate a reset signal to reset a flip flop.

6. **Claim 9** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kubota et al. ( US 6,288,699 B1 ) in view of Yamagishi et al. ( US 2004/0012580 A1 ) and Saito ( US 20010054924 A1 ), as applied to Claim 8, in view of Takuwa ( US 5,793,363 ).

For **claim 9,** Kubota teaches latch failure detector generates a plurality of latch failure detection signals obtained by sequentially delaying said latch failure detection signal by a predetermined

delay amount to generate a logical product of said plurality of latch failure detection signals (Kubota, column 4, lines 1-21, 45-61).

Kubota does not specifically teach a logical product.

However, in the same field of endeavor, Takuwa teaches using the logical product of a latch output (Takuwa, column 7, lines 56-60).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kubota's latch failure detector with Takuma's latch output because the addition of using a logical product could simply the circuitry by requiring less wire to be used, since the output of a logical product can be carried on a single transmission wire.

**Response to Arguments**

7. Applicant's arguments considered, but are respectfully moot in grounds of new rejection.

Applicant is thanked for amending the title of the invention to better describe the invention.

Applicant has amended to better claim the specifics of the driving, as related to a plasma display, as well as better claiming the optimal range.

Most of Applicant's arguments are directed to Kubota's invention being applied to an LCD and not a plasma. In response to this, the rejection has been modified and a new reference, Yamagishi has been added, who teaches of a similar invention to Applicant and Kubota, and who

also notes that it would be obvious to implement such a system in a plasma display. Respectfully, clock timing issues are known in several types of display and Applicant has even noted that the writer period, in which these phase adjustments are being made, are akin to a sustain period of a plasma. Implementing Kubota's driving method in a display device would be obvious in light of the teachings of the Yamagishi reference.

Another change is that Applicant better claimed the optimal range, such as selecting the center of this range. However, and respectfully, one of ordinary skill in the art would realize that selecting the center is always best for optimization purposes and Kubota already teaches of this and is also concerned with finding optimal ranges to avoid latch errors. Please note KSR principles and case law which relate to optimization purposes and that it is not a patentable step given that it is obvious and beneficial to optimize the value to avoid errors.

Applicant is advised to overcome the current rejection by better claiming the optimization process. While some details were added in this amendment, more details from the disclosure can be claimed to differentiate it from the Kubota reference.

**Conclusion**

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DENNIS P. JOSEPH whose telephone number is (571)-270-1459. The examiner can normally be reached on Monday-Friday, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Alexander S. Beck/
Supervisory Patent Examiner, Art Unit 2629

DJ